Amendments to the Claims

This listing of claims will replace all prior versions, and listing, of claims in this application.

Listing of Claims:

1. (Currently amended) A fractional-spaced digital equalizer comprising:

a bank of register delay elements representing a data register bank that stores samples of an input distorted waveform;

a switch (S1) to control a portion of a joint intersymbol interference (ISI)-canceling and matched filter (MF) equalizer update associated with an intersymbol interference (ISI)-cancellation process;

a bank of register elements representing equalizer feedforward (FF) weight register bank that stores equalizer (FF) weights coefficient values;

a bank of multiplier elements used in forming inner products associated with both the (ISI)-cancellation and (MF) constraint updates;

a bank of summing nodes used in forming inner products associated with both the (ISI)-cancellation and (MF) constraint updates;

an (M:1) commutation device to perform decimation to the symbol rate;

an algorithm to form the error sequence associated with (ISI) cancellation;

an algorithm to convert an (ISI) cancellation error signal into an adjustment signal needed to control an equalizer (FF) weight update in accordance with a criterion for (ISI) cancellation;

an algorithm to update the contents of the equalizer (FF) weight register bank in accordance with first, the criterion for (ISI)-cancellation, and second, a (MF) constraint criterion;

a bank of register elements representing the constraint register bank to store samples of the constraint waveform;

an algorithm that generates samples of the constraint waveform;

the constraint waveform used in forming the inner product associated with the (MF) constraint processing;

a switch (S2) to control that portion of the joint (ISI)-canceling and (MF) equalizer update associated with the (MF) constraint process;

a parameter (β) representing the constraint level of the (MF) constraint update;

a differencing node to subtract the orthogonality measure from the constraint level in order to form the constraint error; and

an algorithm to convert the constraint error signal into an adjustment signal needed to control the equalizer (FF) weight update in accordance with the (MF) constraint criterion[;].

2. (previously presented) The fractional-spaced equalizer as set forth in claim 1 wherein said equalizer operates at M-samples-per-symbol where M > 1 and satisfies the Nyquist Criterion.

3. (currently amended) The fractional-spaced equalizer as set forth in claim 2 wherein said sampling factor M is equal to 2.

4. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said equalizer operates as a complex equalizer comprising complex operations[;].

5. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said equalizer operates as a real equalizer comprising real operations[;].

6. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein the signal occurring prior to said M-to-1 decimator is passed directly to switch S2, instead of passing through said M-to-1 commutator, so that constraint processing can be performed using every fractional-spaced sample of the distorted input waveform[;]_.

7. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm that computes the error associated with ISI-cancellation is based upon a training sequence update and comprises:

a training sequence of distortion-less data; and

a differencing node to form the difference between the equalized decimated signal and the training sequence[;]_.

8. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm that computes the error associated with (ISI)_ cancellation is based upon a decision-directed update and comprises:

a slicer device to quantize samples of equalized decimated signal; and

a differencing node to form the difference between pre-slicer sequence and post-slicer sequence[;].

9. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm that computes the error associated with (ISI) cancellation is based upon a blind constant modulus algorithm (CMA) update and comprises:

an algorithm to form the statistical parameter (R_m) measuring the ratio o(f moments of the pre-pulse shaped modulation amplitudes;

a switch (S7) to eliminate the computation of (R_m) from the processing so that parameter (R_m) is computed only one time;

a register element to store the value of parameter (R_m);

a complex conjugation operator to conjugate the sample input to the (CMA);

a multiplier element to obtain the product between the input sample and its complex conjugate;

a differencing node to form the difference between parameter (R_m) and the absolute value of the input sample squared; and

a multiplier element to obtain the product of (1) the difference between parameter (R_m) and the absolute value of the input sample squared and (2) the input sample[;].

10. (currently amended) The fractional-spaced equalizer as set forth in claim 9 wherein said algorithm forming the value (R_m) comprises:

an absolute value operator to perform an absolute value of the input modulated 2-tuple;

a divide operation to form the value of (R_m);

a switch (S8) to control when the numerator portion of a ratio is to be delivered to the divide operation to form the value of parameter (R_m);

a switch (S9) to control when the denominator portion of a ratio is to be delivered to the divide operation to form the value of parameter (R_m);

a counter to control when switches (S8) and (S9) are closed to form the value of parameter (R_m);

a summing node used in the ratio's numerator accumulation process;

a summing node used in the ratio's denominator accumulation process;

a register element used in the ratio's numerator accumulation process;

a register element used in the ratio's denominator accumulation process;

a squaring operator;

a operator to perform a power operation to the m-th power; and

a parameter (m) representing the statistical moment of

the (CMA) update satisfies the condition m > 0[;].

11. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm converting the (ISI) cancellation error signal into an adjustment signal comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input error sequence;

a parameter (μ) to control the adaptation rate of the equalizer's weight in accordance with the criterion for (ISI) cancellation; and

a multiplier element to form the product of the conjugated error sequence and parameter (μ)[;].

12. (currently amended) The fractional-spaced equalizer as set forth in claim 11 wherein the value for said scalar (μ) is in the range $0 < \mu < \mu_{crit}$ and μ_{crit} is inversely proportional to the power level of the samples residing in the equalizer data register bank[;].

13. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm driving the equalizer weight update comprises:

a bank of multiplier elements to scale each element in the data register bank with a sample of the (ISI) cancellation adjustment signal; and

a bank of summing nodes to form the addition of the said bank of products with the current contents of the equalizer weight register bank[;].

14. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein constraint waveform is defined to be a high frequency signal[;].

15. (currently amended) The fractional-spaced equalizer as set forth in claim 14 wherein said high frequency signal representing said constraint waveform is sinusoidal in nature[;].

16. (currently amended) The fractional-spaced equalizer as set forth in claim 15 wherein said high frequency sinusoid signal is a complex sinusoid of the form A exp{ j 2π f kT_s + ϕ }[;].

17. (currently amended) The fractional-spaced equalizer as set forth in claim 16 wherein said frequency (f) is a time variable frequency[;].

18. (currently amended) The fractional-spaced equalizer as set forth in claim 17 wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the (FSE) that is comparable to that of a (MF).

19. (currently amended) The fractional-spaced equalizer as set forth in claim 16 wherein said amplitude (A) is an amplitude fixed to a singular value and satisfies $|A| > 0$[;].

20. (currently amended) The fractional-spaced equalizer as set forth in claim 16 wherein said amplitude (A) is a time variable amplitude (A_{e}) and satisfies $|A| > 0$[;].

21. (currently amended) The fractional-spaced equalizer as set forth in claim 16 wherein said phase (ϕ) is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$[;].

22. (currently amended) The fractional-spaced equalizer as set forth in claim 16 wherein said phase (ϕ) is a time variable phase and satisfies {$0 \leq \phi < 2\pi$}[;].

23. (previously presented) The fractional-spaced equalizer as set forth in claim 15 wherein said high frequency sinusoid signal is a real sinusoid, either of the form A sin{ 2π f $kT_s + \phi$ } or A cos{ 2π f $kT_s + \phi$}.

24. (currently amended) The fractional-spaced equalizer as set forth in claim 23 wherein said frequency (f) of said sinusoid is a time variable frequency[;].

25. (currently amended) The fractional-spaced equalizer as set forth in claim 24 wherein minimum and maximum values of said time-variable frequency (f) are selected to develop a robust out-of-band spectral mask for the (FSE) that is comparable to that of a (MF).

26. (currently amended) The fractional-spaced equalizer as set forth in claim 23 wherein said amplitude (A) is an amplitude fixed to a singular value and satisfies $|A| > 0$[;].

27. (currently amended) The fractional-spaced equalizer as set forth in claim 23 wherein said amplitude (A) is a time variable amplitude ($A_{s)}$ and satisfies $|A| > 0$;

28. (currently amended) The fractional-spaced equalizer as set forth in claim 23 wherein said phase (ϕ) is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$[;].

29. (currently amended) The fractional-spaced equalizer as set forth in claim 23 wherein said phase (ϕ) is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$[;].

30. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said algorithm generating said constraint waveform comprises:

an overflow counter to generate an integer (i) that indexes a frequency register bank;

a frequency register bank storing the independent frequencies of the sinusoidal signal representing the constraint waveform;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a parameter (N) representing the number of independent constraint frequencies;

a summing node to increment the count of the overflow counter; and

a quadrature oscillator that generates samples of the sinusoidal signal representing the constraint waveform from the frequencies in the frequency register bank[;].

31. (currently amended) The fractional-spaced equalizer as set for in claim 1 wherein samples of said constraint waveform are loaded into the constraint register bank via (ROM) lookup table[;].

32. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein value of said constraint level parameter (β) resides in the range {0 ≤ β < 1}.

33. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said differencing node forming constraint error is eliminated from the architecture of the present invention when parameter (β) is set to 0.

34. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein said (MF) error adjustment algorithm comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input MF constraint error;

a parameter (α) to control the adaptation rate of the equalizer's weight in accordance with the (MF) constraint criterion; and

a multiplier element to form the product of the complex conjugate (MF) constraint error and parameter (α)[;].

35. (currently amended) The fractional-spaced equalizer as set forth in claim 34 wherein the value for a scalar (α) satisfies α > 0;

36. (currently amended) The fractional-spaced equalizer as set forth in claim 34 wherein the value for said scalar (a) is equal to A/L commensurate with the constraint waveform defined as a sinusoidal signal of amplitude (A) and length (L)[;].

37. (previously presented) The fractional-spaced equalizer as set forth in claim 1 where a fractional-spaced equalizer further comprises an algorithm that modifies the constraint waveform via time domain windowing;

38. (currently amended) The fractional-spaced equalizer as set forth in claim 36 wherein said algorithm that modifies the constraint waveform via time domain windowing does so with a single window function[;].

39. (currently amended) The fractional-spaced equalizer as set forth in claim 38 wherein said algorithm that modifies the constraint waveform via time domain windowing with a single window function comprises:

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a window function;

a set of coefficients representing a window function used to window the samples of the constraint sinusoid; and

a bank of register elements to store the set of coefficients representing the window function[;]_.

40. (currently amended) The fractional-spaced equalizer as set forth in claim 39 wherein said window function is derived from any function that can modify the time response of the constraint sinusoid through time-domain windowing[;]_.

41. (currently amended) The fractional-spaced equalizer as set forth in claim 40 wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function[;]_.

42. (currently amended) The fractional-spaced equalizer as set forth in claim 37 wherein said algorithm that modifies the constraint waveform via time domain windowing does so with multiple window functions[;]_.

43. (currently amended) The fractional-spaced equalizer as set forth in claim 42 wherein said algorithm that modifies the constraint waveform via time domain windowing with multiple window functions comprises:

a register bank to store the samples of the current state of the windowed constraint waveform during the multi-window process;

a switch (S10) to load the pre-windowed constraint waveform into the register bank only one time;

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a particular window function of the set of window functions;

a collection of window functions used to window the samples of the constraint sinusoid;

a collection of banks of register elements to store the set of coefficients of the collection of window functions;

a switch (S12) to allow the multiplier bank to access a particular window function of the set of window functions; and

a switch (S11) to deliver the windowed constraint waveform to the constraint register bank when the windowing process has been completed[;].

44. (previously presented) The fractional-spaced equalizer as set forth in claim 43 wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function.

45. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein a fractional spaced equalizer further comprises an algorithm that controls the rate at which the contents of the equalizer's (FF) weight register bank are updated in accordance with the (MF) constraint update[;].

46. (currently amended) The fractional-spaced equalizer as set forth in claim 45 where said algorithm that controls the rate at which the contents of the equalizer's (FF) weight register bank are updated in accordance with the (MF) constraint criterion comprises:

a switch (S3) to control when the algorithm for updating the contents of the equalizer (FF) weight registers is to be engaged;

an overflow counter to control when switch (S3) is to be open and closed;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

a summing node to increment the count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a switch (S4) to allow the overflow test to use the value designated by parameter (P0) as the maximum count value;

a switch (S5) to allow the overflow test to use the value designated by parameter (P1) as the maximum count value;

a switch (S6) to allow the overflow test to use the value designated by parameter (P2) as the maximum count value;

a parameter (P0) that represents a maximum count value;

a parameter (P1) that represents a maximum count value; and

a parameter (P2) that represents a maximum count value[;].

47. (currently amended) The fractional-spaced equalizer as set forth in claim 46 wherein said parameter (P0), (P1), and (P2) are integers and satisfy P0 > 0, P1 > 0, and P2 > 0[;].

48. (currently amended) The fractional-spaced equalizer as set forth in claim 1 wherein a fractional spaced equalizer further comprises an algorithm that initializes the contents of the equalizer's (FF) weight register bank with coefficients of square root raised cosine (RRC) (MF) [;].

49. (currently amended) The fractional-spaced equalizer as set forth in claim 48 where said algorithm that initializes the contents of the equalizer's (FF) weight register bank with coefficients of a (RRC) (MF) comprises:

a selected set of (RRC) (MF) coefficients loaded from (ROM) into the register positions of the equalizer (FF) weight register bank; and

a switch (S13) to shutoff the initialization after the contents of the equalizer (FF) weight register bank[;].

50. (previously presented) The fractional-spaced equalizer as set forth in claim 1 wherein a fractional-spaced equalizer further comprises a decision-feedback update.

51. (currently amended) The fractional-spaced equalizer as set forth in claim 50 where said decision-feedback update comprises:

a register delay bank to store past decisions from a slicer device;

a slicer device to quantize samples of equalized decimated signal;

a register bank representing the decision register bank that stores the values of the weights of a decision-feedback filter;

a bank of multiplier elements used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a bank of summing nodes used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a single summing node adding the decision register and decision-feedback weight inner product to the output of the M:1 commutator;

a bank of multiplier elements used in updating the contents of the decision-feedback weight register bank;

a bank of summing nodes in updating the contents of the decision-feedback weight register bank[;].

52. (canceled)

53. (currently amended) A fractional-spaced digital equalizer comprising:

a set of (M) banks of register delay elements representing data sub-register banks (u_0, u_1, .. … $u_{(M-1)}$) that store samples of the input distorted waveform which are commutated to data sub-register banks (u_0, u_1, …, $u_{(M-1)}$);

a set of (M) banks of register elements representing an equalizer (FF) weight sub-register banks (w_0, w_1, …, $w_{(M-1)}$) that store the values of the equalizer's (FF) weights, with each bank storing a different subset of the total weight set;

a set of (M) banks of register elements representing constraint sub-register banks (c_0, c_1, $c_{(M-1)}$) that store samples of a constraint waveform;

an algorithm that generates samples of the constraint waveform;

the constraint waveform used in forming the inner product associated with the (MF) constraint processing;

a commutator (COM 1) which delivers samples of the

input distorted waveform to be equalized to data sub-register banks (u_0, u_1, … $u_{(M-1)}$);

a switch (S1) to control a portion of a joint (ISI)-canceling and (MF) equalizer update associated with the (ISI)-cancellation process;

a bank of multiplier elements used in forming inner products associated with both the (ISI)-cancellation and (MF) constraint updates;

a bank of summing nodes used in forming inner products associated with both the (ISI)-cancellation and (MF) constraint updates;

a single register delay element to store inner products associated with the formation of the equalized signal;

a switch (S14) to control when an error sequence associated with (ISI)-cancellation is to be developed;

a switch (S2) to control a portion of the time-multiplexing process associated with the (MF) constraint update;

a single register delay element to store an inner product computation associated with a (MF) constraint process;

a switch (S15) to control when a (MF) constraint error is to be developed;

a commutator (COM 2) which controls which pair of sub-register banks, either $\{\underline{u}_0, \underline{c}_0\}$ or $\{\underline{u}_1, \underline{c}_1\}$ or $\{\underline{u}_{(M-1)}, \underline{c}_{(M-1)}\}$, are to access the multiplier bank at the current (COM 1) position;

a commutator (COM 3) which controls which equalizer (FF) weight sub-register bank, either (w_0 or w_1 or $w_{(M-1)}$) is to access the multiplier bank at the current (COM 1) position;

a clock to control an adjustment of (COM 1), (COM 2), and (COM 3);

a summing node to add the two inner product sums which form the equalized signal;

an algorithm to form the error sequence associated with (ISI) cancellation;

an algorithm to convert the (ISI) cancellation error signal into an adjustment signal needed to control an equalizer (FF) weight update in accordance with a criterion for (ISI) cancellation;

an algorithm to update the contents of the equalizer (FF) weight sub-register banks $\{\underline{w}_0, \underline{w}_1, \cdots, \underline{w}_{(M-1)}\}$ in accordance with first, the criterion for (ISI)-cancellation, and second, an (MF) constraint criterion;

a summing node to add the two inner product sums which form a measure of orthogonality between the equalizer's weights and constraint (

a parameter (β) representing a constraint level of the (MF) processing;

a differencing node needed to subtract the orthogonality measure from the constraint level in order to form the constraint error;

an algorithm to convert the constraint error signal into an adjustment signal needed to control the equalizer FF weight update in accordance with the _(MF)_ constraint criterion.

54. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein a poly-phase configured equalizer accommodates an input signal sampled at _(M)_-samples-per-symbol by using _(M)_ data sub-register banks, _(M)_ constraint register sub-banks, and _(M)_ equalizer _(FF)_ weight register banks.

55. (currently amended) The fractional-spaced equalizer as set forth in claim 54 wherein said sampling factor _(M)_ is equal to 2[;]_.

56. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said equalizer operates as a complex equalizer comprising complex operations[;]_.

57. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said equalizer operates as a real equalizer comprising real operations[;]_.

58. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said algorithm that computes the error associated with (ISI) cancellation is based upon a training sequence update and comprises:

a training sequence of distortion-less data; and

a differencing node to form the difference between the equalized decimated signal and the training sequence[;].

59. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said algorithm that computes the error associated with (ISI) cancellation is based upon a decision-directed update and comprises:

a slicer device to quantize samples of equalized decimated signal; and

a differencing node to form the difference between pre-slicer sequence and post-slicer sequence[;].

60. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said algorithm that computes the error associated with (ISI) cancellation is based upon a blind (CMA) update and comprises:

an algorithm to form the statistical parameter (R_m) measuring the ratio of moments of the pre-pulse shaped modulation amplitudes;

a switch (S7) to eliminate the computation of (R_m) from the processing so that parameter (R_m) is computed only one time;

a register element to store the value of parameter (R_m);

a complex conjugation operator to conjugate the sample input to the (CMA);

a multiplier element to obtain the product between the input sample and its complex conjugate;

a differencing node to form the difference between parameter (R_m) and the absolute value of the input sample squared; and

a multiplier element to obtain the product of (1) the difference between parameter (R_m) and the absolute value of the input sample squared and (2) the input sample.

61. (currently amended) The fractional-spaced equalizer as set forth in claim 60 wherein said algorithm forming the value (R_m) comprises:

an absolute value operator to perform an absolute value of the input modulated 2-tuple;

a divide operation to form the value of (R_m);

a switch (S8) to control when the numerator portion of a ratio is to be delivered to the divide operation to form the value of parameter (R_m);

a switch (S9) to control when the denominator portion of a ratio is to be delivered to the divide operation to form the value of parameter (R_m);

a counter to control when switches (S8) and (S9) are closed to form the value of parameter (R_m);

a summing node used in the ratio's numerator accumulation process;

a summing node used in the ratio's denominator accumulation process;

a register element used in the ratio's numerator accumulation process;

a register element used in the ratio's denominator accumulation process;

a squaring operator;

an operator to perform a power operation to the (m-th) power; and

a parameter (m) representing the statistical moment of the (CMA) update satisfies the condition (m) > 0[;].

62. (currently amended) The fractional-spaced equalizer as set forth in claim 54 wherein said algorithm converting the (ISI) cancellation error signal into an adjustment signal comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input error sequence;

a parameter (μ) to control the adaptation rate of the equalizer's weight in accordance with the criterion for (ISI) cancellation; and

a multiplier element to form the product of the conjugated error sequence and parameter (μ) [;].

63. (currently amended) The fractional-spaced equalizer as set forth in claim 62 wherein the value for said parameter (μ) is in the range $0 < (\mu < \mu_{crit})$ and (μ_{crit}) is inversely proportional to the power level of the samples of distorted waveform residing in the equalizer data register bank.

64. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said algorithm driving the equalizer weight update comprises:

a bank of multiplier elements to scale each element in the data register bank with a sample of the _(ISI)_ cancellation adjustment signal; and

a bank of summing nodes to form the addition of the said bank of products with the current contents of the equalizer weight register bank[;]_.

65. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein constraint waveform is defined to be a high frequency signal[;]_.

66. (currently amended) The fractional-spaced equalizer as set forth in claim 65 wherein said high frequency signal representing said constraint waveform is sinusoidal in nature[;]_.

67. (currently amended) The fractional-spaced equalizer as set forth in claim 66 wherein said high frequency sinusoid signal is a complex sinusoid of the form $A \exp\{ j 2\pi f kT_s + \phi \}$[;]_.

68. (currently amended) The fractional-spaced equalizer as set forth in claim 67 wherein said frequency (f) is a time variable frequency[;].

69. (currently amended) The fractional-spaced equalizer as set forth in claim 68 wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the (FSE) that is comparable to that of a (MF)[;].

70. (currently amended) The fractional-spaced equalizer as set forth in claim 67 wherein said amplitude (A) is an amplitude fixed to a singular value and satisfies $|A| > 0$[;].

71. (currently amended) The fractional-spaced equalizer as set forth in claim 67 wherein said amplitude (A) is a time variable amplitude and satisfies $|A| > 0$[;].

72. (currently amended) The fractional-spaced equalizer as set forth in claim 67 wherein said phase (ϕ) is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$[;].

73. (currently amended) The fractional-spaced equalizer as set forth in claim 67 wherein said phase (ϕ) is a time variable phase and satisfies {$0 \leq \phi < 2\pi$}[;].

74. (currently amended) The fractional-spaced equalizer as set forth in claim 66 wherein said high frequency sinusoid signal is a real sinusoid, either of the form A sin{ 2π f $kT_s + \phi$ } or A cos{ 2π f $kT_s + \phi$ }[;].

75. (currently amended) The fractional-spaced equalizer as set forth in claim 74 wherein said frequency (f) of said sinusoid is a time variable frequency[;].

76. (currently amended) The fractional-spaced equalizer as set forth in claim 75 wherein minimum and maximum values of said time-variable frequency are selected to develop a robust out-of-band spectral mask for the (FSE) that is comparable to that of a MF[;].

77. (currently amended) The fractional-spaced equalizer as set forth in claim 74 wherein said amplitude (A) is an amplitude fixed to a singular value and satisfies $|A| > 0$[;].

78. (currently amended) The fractional-spaced equalizer as set forth in claim 74 wherein said amplitude (A) is a time variable amplitude and satisfies $|A| > 0$[;].

79. (currently amended) The fractional-spaced equalizer as set forth in claim 74 wherein said phase (ϕ) is a phase fixed to a singular value and satisfies $\{0 \leq \phi < 2\pi\}$[;].

80. (currently amended) The fractional-spaced equalizer as set forth in claim 74 wherein said phase (ϕ_s) is a time variable phase and satisfies $\{0 \leq \phi < 2\pi\}$[;].

81. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein a sinusoid representing said constraint waveform is generated via an algorithm comprising of:

an overflow counter to generate an integer (i) that indexes a frequency register bank;

a frequency register bank storing the independent frequencies of the sinusoidal signal representing the constraint waveform;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a parameter (N) representing the number of independent constraint frequencies;

a summing node to increment the count of the overflow counter; and

a quadrature oscillator that generates samples of the sinusoidal signal representing the constraint waveform from the frequencies in the frequency register bank.

82. (previously presented) The fractional-spaced equalizer as set forth in claim 53 wherein samples of a sinusoidal constraint waveform are loaded into the constraint register bank via ROM lookup table.

83. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein value of said constraint level parameter (β) resides in the range {0 ≤ β < 1}[;].

84. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said differencing node forming constraint error is eliminated from the architecture of the present invention when a parameter (β) is set to 0.

85. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein said (MF) error adjustment algorithm comprises:

a complex conjugation operator to perform a complex conjugation of the samples of input (MF) constraint error;

a parameter (α) to control the adaptation rate of the equalizer's weight in accordance with the (MF) constraint criterion; and

a multiplier element to form the product of the complex conjugate (MF) constraint error and parameter (α)[;].

86. (currently amended) The fractional-spaced equalizer as set forth in claim 85 wherein the value for a scalar (α) satisfies $\alpha > 0$.

87. (currently amended) The fractional-spaced equalizer as set forth in claim 86 wherein the value for said scalar (α) is equal to (A /L) commensurate with the constraint waveform defined as a sinusoidal signal of amplitude (A) and length (L)[;].

88. (previously presented) The fractional-spaced equalizer as set forth in claim 53 wherein a fractional-spaced equalizer further comprises an algorithm that modifies the constraint waveform via time-domain windowing.

89. (currently amended) The fractional-spaced equalizer as set forth in claim 88 wherein said algorithm that modifies the constraint waveform via time-domain windowing does so with a single window function[;].

90. (currently amended) The fractional-spaced equalizer as set forth in claim 89 wherein said algorithm that modifies the constraint waveform via time domain windowing with a single window function comprises:

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a window function; and

a set of coefficients representing a window function used to window the samples of the constraint sinusoid; and

a bank of register elements to store the set of coefficients representing the window function[;].

91. (currently amended) The fractional-spaced equalizer as set forth in claim 90 wherein said window function is derived from any function that can modify the time response of the constraint sinusoid through time-domain windowing[;].

92. (currently amended) The fractional-spaced equalizer as set forth in claim 91 wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function[;].

93. (previously presented) The fractional-spaced equalizer as set forth in claim 88 wherein said algorithm that modifies the constraint waveform via time domain windowing does so with multiple window functions.

94. (currently amended) The fractional-spaced equalizer as set forth in claim 93 wherein said an algorithm that modifies the constraint waveform via time domain windowing with multiple window functions comprises:

a register bank to store the samples of the current state of the windowed constraint waveform during the multi-window process;

a switch (S10) to load the pre-windowed constraint waveform into the register bank only one time;

a bank of multiplier elements used to multiply each sample of the time series of each constraint sinusoid with a particular window function of the set of window functions;

a collection of window functions used to window the samples of the constraint sinusoid;

a collection of banks of register elements to store the set of coefficients of the collection of window functions;

a switch (S12) to allow the multiplier bank to access a particular window function of the set of window functions; and

a switch (S11) to deliver the windowed constraint waveform to the constraint register bank when the windowing process has been completed[;].

95. (currently amended) The fractional-spaced equalizer as set forth in claim 94 wherein said window function is derived from a rectangular, Bartlett, Blackman, Chebyshev, hamming, hann, Kaiser, or triangular window function[;].

96. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein a fractional spaced equalizer further comprises an algorithm that controls the rate at which the contents of the equalizer's (FF) weight register bank are updated in accordance with the (MF) constraint update.

97. (currently amended) The fractional-spaced equalizer as set forth in claim 96 where said algorithm that controls the rate at which the contents of the equalizer's (FF) weight register bank are updated in accordance with the (MF) constraint update comprises:

a switch (S3) to control when the algorithm for updating the contents of the equalizer (FF) weight registers is to be engaged;

an overflow counter to control when switch (S3) is to be open and closed;

a scalar set to value of 1.0;

a register that stores the state of the incremental count of the overflow counter;

a summing node to increment the count of the overflow counter;

an overflow test to compare the value in the register with a parameter representing a maximum count value;

a switch (S4) to allow the overflow test to use the value designated by parameter (P0) as the maximum count value;

a switch (S5) to allow the overflow test to use the value designated by parameter (P1) as the maximum count value;

a switch (S6) to allow the overflow test to use the value designated by parameter (P2) as the maximum count value;

a parameter (P0) that represents a maximum count value;

a parameter (P1) that represents a maximum count value; and

a parameter (P2) that represents a maximum count value[;].

98. (currently amended) The fractional-spaced equalizer as set forth in claim 97 wherein said parameters (P0), (P1), and (P2) are integers and satisfy (P0) > 0, (P1) > 0, and (P2) > 0[;].

99. (currently amended) The fractional-spaced equalizer as set forth in claim 53 wherein a fractional spaced equalizer further comprises an algorithm that initializes the contents of the equalizer's (FF) weight register bank with coefficients of (RRC) (MF).

100. (currently amended) The fractional-spaced equalizer as set forth in claim 99 where said algorithm that initializes the contents of the equalizer's (FF) weight register bank with coefficients of a (RRC) (MF) comprises:

a selected set of (RRC) (MF) coefficients loaded from (ROM) into the register positions of the equalizer (FF) weight register bank; and

a switch (S13) to shutoff the initialization after the contents of the equalizer FF weight register bank[;].

101. (previously presented) The fractional-spaced equalizer as set forth in claim 53 wherein a fractional-spaced equalizer further comprises a decision-feedback update.

102. (currently amended) The fractional-spaced equalizer as set forth in claim 101 where said decision-feedback update comprises:

a register delay bank to store past decisions from a slicer device;

a slicer device to quantize samples of equalized decimated signal;

a register bank representing the decision register bank that stores the values of the weights of a decision-feedback filter;

a bank of multiplier elements used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a bank of summing nodes used in forming the inner product between the contents of the decision register bank and the decision-feedback weight register bank;

a single summing node adding the decision register and decision-feedback weight inner product to the output of the 2:1 commutator;

a bank of multiplier elements used in updating the contents of the decision-feedback weight register bank; and

a bank of summing nodes in updating the contents of the decision-feedback weight register bank[;]_

103. Cancelled.